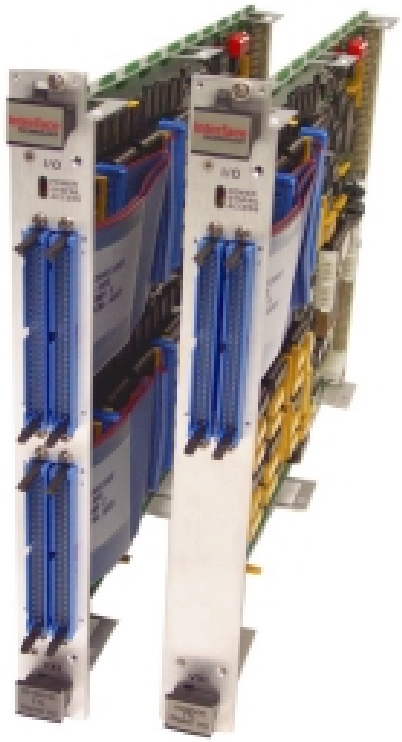
IO50 and IO100
Digital I/O Modules



- Up to 128 I/O Channels per Module
- Multiple Modules Can be Synchronously Triggered
- On-board Processor for Autonomous Operation
- Memory Backed Pins for Timing or Handshake Controlled Inputs or Outputs
- TTL, CMOS, TTL Open Collector, Differential TTL, or Switched HV Outputs
- Latched Inputs and Double Latched Outputs Allow Simultaneous Reads or Writes on Any Size and Number of Fields
- Message-based SCPI Commands and Software Drivers for Easy Test Program Development
- VXI Memory Mapped Registers for High Speed Register-based Operation
- User Defined Data Fields From 1-bit to 32-bits Wide
- Byte Available, Byte Request, Data Valid, Data Acknowledge and 4 Tristate Control Lines per I/O Connector
- User Configurable I/O Termination
- Space For User Supplied Mezzanine Board Allows Custom I/O Drivers

Description

The IO50 and IO100 Digital Input/Output modules are used in process control, microprocessor cycle emulation, bus cycle emulation, process simulation and functional board or circuit test applications. The IO100 provides up to 128 channels of digital I/O; the IO50 providing up to 64 channels of digital I/O. Each group of 8 channels may be software configured as either input or output. Tristate control of outputs allow for emulation of bidirectional data and control buses. Four 50-pin IDC connectors are provided on the IO100 front panel; two on the IO50. Each I/O connector provides (32) I/O channels, (4) I/O handshake strobes, and (4) tristate control/output enable inputs.

All modules use high level, SCPI compatible commands for setup and control of I/O channels. They also support VME dual-ported RAM and registers. I/O pins can be programmed with high-level commands or direct, high speed VME read/writes, the same as used for register-based instruments. This combination of programming formats results in both worlds high functionality and high speed.

Memory emulation and block I/O modes allow autonomous operation from the local microprocessor. Data fields may be programmed from 1-bit to 32-bits wide. Multiple data fields may be defined, allowing I/O pins to be grouped together based on function. Double latching the outputs allows all output channels to transition at the same time regardless of field size or the number of fields defined. Latching the inputs allows a full 128-bit wide read with a single command (64 channels for the IO50). Utilizing the VXITTLTRG lines, modules can be linked together for even wider I/O channel groups.

The IO53 and IO130 use 32 or 64 output channels to drive 30 or 60 optically isolated solid state relays. This allows the modules to control high voltage applications up to 100 volts. Switched voltages can be user supplied or selected from +5, ± 12 , and ± 24 volts available from the VXI backplane. Both modules use a mezzanine board to provide the switched high voltage outputs. Other input and output logic formats can be supported by means of user supplied mezzanine boards.

The IO54 and IO140 modules are the latest additions to the IO50 / IO100 family. The IO54 provides 32 Differential TTL I/O channels, each provided with a switchable 100 ohm termination. The IO140 provides 32 differential I/O channels with switchable 100 ohm terminations, plus 64 TTL or CMOS I/O channels or 64 differential I/O channels. Differential I/O channels meet RS-422-A standard. Both modules support external I/O handshaking. IO140 TTL channels are the same as the IO100 TTL channels described above.

Ten Models to Choose From

Model	I/O Channels	Logic Family
IO50	64	FTTL
IO51	64	ACTTTL/CMOS
IO52	64	TTL Open Collector
IO53	30 Outputs + 32	Solid State Relay + FTTL or CMOS I/O
IO54	32 Diff. I/O	Differential TTL
IO100	128	FTTL
IO110	128	ACTTTL/CMOS
IO120	128	TTL Open Collector
IO130	30 Outputs + 96 or 60 Outputs + 64	Solid State Relay + FTTL or CMOS I/O
IO140	32 Diff. I/O + 64 TTL or CMOS I/O or 64 Diff. I/O	Differential TTL + TTL or CMOS

*IO50/IO100 SPECIFICATIONS**

Logic Families:

FTTL	Vol*	0.55 V	Voh**	2.4 V
IO100/IO50	Vil	0.8 V	Vih	2.0 V
	Iol	64 mA	Ioh	-3 mA
Skew****	15 ns, max.			
Rise/Fall	3 ns/3 ns			
CMOS	Vol*	0.5 V	Voh**	3.7 V
IO110/IO51	Iol	24 mA	Ioh	-24 mA
Skew****	20 ns, max.			
Rise/Fall	4 ns/4 ns			
Open Collector	Vol*	0.42 V	Voh**	5.0 V
IO120/IO52	Vil	0.8 V	Vih	2.0 V
	Iol	64 mA	Ioh***	0.5 mA
Skew****	20 ns, max.			
Rise/Fall	3 ns			
Switched				
IO130/IO53				
Max Voltage	100 V peak AC/DC			
Turn on/off Time	4 ms			
On Resistance	20 ohm max.			
Isolation	Optical, 3750 V			
Carry Current	120 mA			
Differential TTL	Vol*	0.50 V	Voh**	2.5 V
IO140/IO54	Vil	0.8 V	Vih	2.0 V
	Iol	20 mA	Ioh	-20 mA (max)
Skew****	21 ns, max.			
Rise/Fall	14 ns/14 ns (typical)			

Handshake and Control:

(except Switched High Voltage Outputs)

Byte Available/Request	Per I/O connector
Data Valid/Acknowledge	Per I/O connector
Tristate Control Inputs	1 per byte (except IO120/IO52)
Output Enable Inputs	1 per byte (IO120/IO52 only)

VXI Specifications

Interface Compatibility:

Type	Message-based, servant only
VXI Revision	1.3 and 1.4
Size	C-size, single slot
Configuration	Static or Dynamic
Interrupt Level	Programmable 1-7
TTLTRG 0-7	Input or output, selectable in groups of two
Memory	A24 RAM, 256K

Power Requirements:

All modules (except IO53/130)	+5 volts, 3.2 A, 16 W typ.
IO53 / IO130	+5 volts, 3.7 A, 18 W typ., ±12, ±24 volts user selectable

Cooling Requirements:

Per-slot Average	16 W typical
Airflow	1L / sec @ 0.30 mm water pressure for 10º C temperature rise

Environmental Specifications:

Temperature	Storage = -40º C to +75º C Operating = 0º C to 45º C
Humidity	5% to 95% relative, noncondensing

Software Drivers:

National Instruments	LabWindows/CVI

* Maximum voltage at minimum load.
** Minimum voltage at maximum load.
*** Depends on pull-up resistor value.
**** Channel-to-channel skew. Add 50 ns for channel-to-channel skew across multiple cards.

*Specifications subject to change without notice.

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